PE Sound Synthesiser 10

KEYBOARD

With these added units the keyboard becomes a unique musical instrument . . .

WHEN the Sound Synthesiser was originally presented for publication it was the intention that it should be classed as a general purpose instrument which could be exploited in the widest possible number of ways and yet retain a basic simplicity of design and ease of construction. During the course of the series however many readers have commented that the musical capabilities of the instrument have been severely restricted by the lack of logarithmic v.c.o.s and thus the oscillator to be described in this article has been included in the keyboard unit in the hope that it will put matters right.

Prospective constructors should note that although the logarithmic v.c.o. is based on the linear v.c.o. which was described in Part 3, the parameters of operation are quite different and the setting-up is rather more critical if it is desired to operate the device within the limitations of a precise range of control voltages.

Although limited to about 11 octaves range with the design values given, it is possible to adjust the operating points to cover a much wider bandwidth. The prototype has operated quite happily from less than 1Hz to greater than 150kHz with a control voltage swing of about 11V and there is no reason to suppose that it could not reach 1MHz, or greater, if the integrator output voltage were to be reduced and a faster comparator employed. As a result it is possible that the oscillator may be suitable for a number of applications outside the sphere of sound synthesis.

The v.c.o. is shown in block schematic form in Fig. 10.1. The control voltage to the oscillator is modified in a differential input summer and then applied to a constant current generator housed in a "transistor oven". The output of the current generator is then led to an integrator/comparator stage through the medium of a current switch which is controlled jointly by the comparator and inverter. The triangular wave output is led to a waveform shaping circuit which provides a sine wave having a very low harmonic content.

DESIGN CONSIDERATIONS

It was decided that the best way of providing a log law performance to the basic v.c.o. outlined in Part 3 of the series was to utilise the entirely predictable logarithmic relationship between the base/emitter voltage (V_{be}) and collector current (I_c) of a bipolar transistor.

. . . Start Here !

This month we start detailing the operation and construction of the keyboard unit for the synthesiser. Regular readers of P.E. who may have been put off by the apparent complexity and/or cost of the synthesiser project as a whole may be interested to learn that the facilities offered by the keyboard unit are such as to allow the instrument to be classed as a music synthesiser in its own right, and at an overall cost of less than £80. Main features of the instrument are as follows:

Two tracking oscillators featuring a variable logarithmic law which allows compatibility with a wide range of control voltages and provides square, triangular and high purity sine wave outputs.

A novel **"floating" divider system** which greatly simplifies tuning the instrument and by means of which the compass of the keyboard can be swung, in tune, from a low frequency of about 6Hz to a high frequency greater than 27kHz. The divider features a switchable "span" facility.

Two modulation amplifiers by means of which the oscillators may frequency modulate one another either separately or at the same time.

Two analogue memory circuits which retain the last programmed divider voltage to either oscillator. Separate portamento controls are incorporated in the hold circuits giving six values of delay from instantaneous to one second.

Two simplified envelope shapers incorporating voltage controlled amplifiers each having a variable Attack and Decay characteristic and featuring a switched percussive attack.

A simple two channel, fixed gain mixer.

Finally, the keyboard divider system incorporates a link switch which allows the two oscillators to be programmed independently by the lower 18 and upper 31 keys respectively. This particular feature greatly improves the "live performance" possibilities. An independent p.s.u. is included.

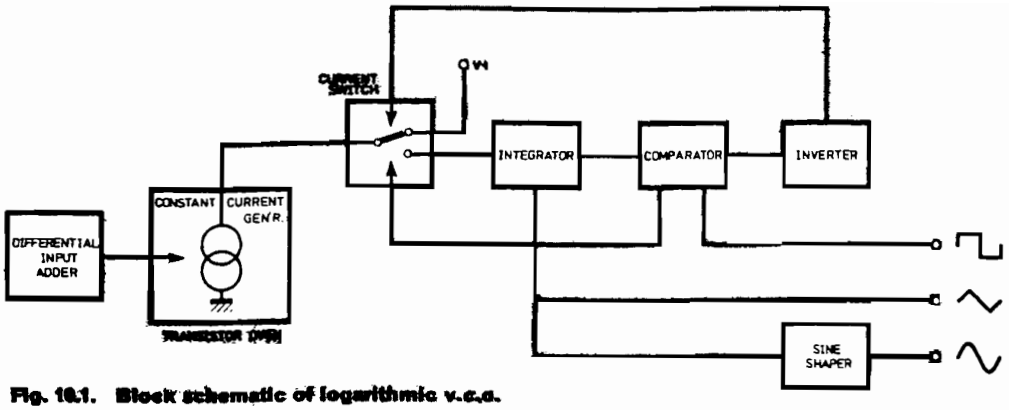


Fig. 10.1. Block schematic of logarithmic v.c.o.

Although the current generator could be almost any discrete transistor the effect of ambient temperature variations would be such as to cause the current demand to vary quite widely and thus adversely affect the "tune" of the oscillator. Consequently it was decided to make use of the inherently close thermal and electrical matching between transistors mounted in a monolithic integrated circuit — the ML3046P and CA3046 both having been tried in the prototype. Extremely close thermal stability is ensured by employing two of the transistors in the array as a heater and sensor respectively and terming the whole arrangement as a "transistor oven."

Fig. 10.2a shows a detailed arrangement of the "oven" while Fig. 10.2b shows the pin connections for the 3046 device. Fig. 10.3 illustrates how the V_{be} of transistors on the array will vary over a wide range of temperatures and provides a guide as to the actual temperature of the chip when the V_{be} of the sensing transistor is known.

In Fig. 10.2a Q1 serves as the heating element while Q2 is used to sense the temperature of the chip. The V_{be} of Q2 is compared with a reference voltage set up by R3, VR1 and R4. The reference voltage will correspond to a temperature which is considerably higher than ambient and will thus be at a lower value than $Q2V_{be}$ when power is first applied. Thus the comparator will switch positive and turn on Q1. As the temperature of the chip rises $Q2V_{be}$ will fall to a point where it is equal to or less than the reference voltage at which time the comparator will switch negative and turn off Q1.

The criteria determining the value of R1 are as follows:—

1. The temperature of the chip must be set considerably above normal ambient conditions (say 40 degrees to 45 degrees Centigrade).

2. The combined power dissipation of Q1 and Q2 must exceed, by a wide margin, the combined power dissipation of the remaining transistors in the array.

3. The current switching of Q1 must not be so violent as to impart a significant jitter to the oscillator waveform.

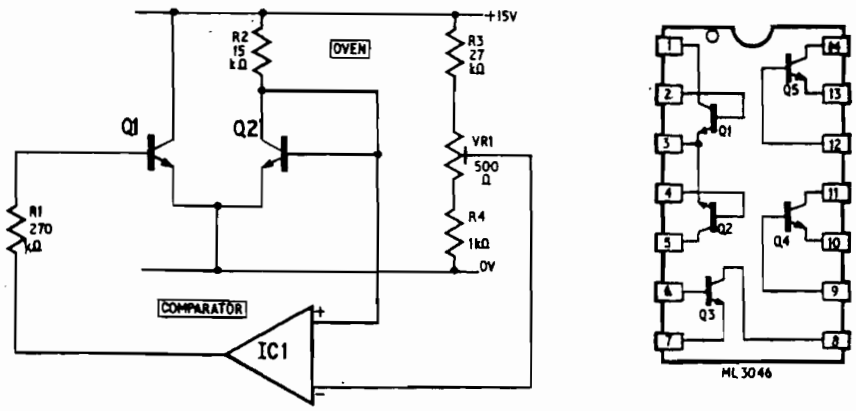


Fig. 10.2(a). Detailed arrangement of the transistor oven; (b) pin connections of the ML3046 and CA3046. Note that pin 13 must be connected to the most negative point in circuit

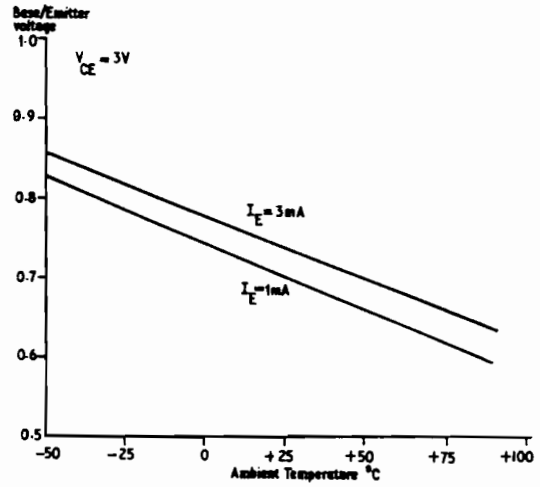


Fig. 10.3. Showing the change in V_{be} for variations in ambient temperature for the ML3046 and CA3046

In practice the value of R1 which gives the closest approach to the above criteria is 270 kilohms. With this value it is possible to set $Q2V_{be}$ to 680mV, that is approximately 45 degrees Centigrade while the combined dissipation of Q1 and Q2 is about 90mW as opposed to the combined dissipation of Q4 and Q5 (the current generators) of about 1·4mW. Detailed setting-up instructions for the "oven" are given later in this article.

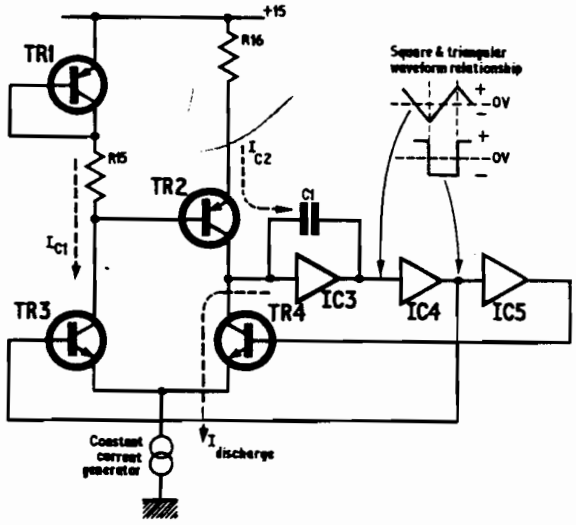


Fig. 10.4. Simplified layout of oscillator section showing operation of current switch

CURRENT SWITCH

Having thus established a thermally stable current generator it now remains to couple this to the input of the v.c.o. In the linear version of the v.c.o. a diode bridge was employed which was switched entirely by the action of the comparator. While this system could no doubt still operate satisfactorily a rather more sophisticated version has been adopted which utilises transistors in place of diodes. The so-called current switch is illustrated in Fig. 10.4. Assuming that the output of IC4 is positive to start with, the operation of the current switch is as follows.

With IC4 positive, the output of IC5 is negative and thus TR3 and TR4 are on and off respectively. With TR3 on the current generator demand will cause a drain across R15 and thus make the base of TR1 more negative than its emitter. TR1 will then turn on in proportion to the demand of the current generator and a current flow I_{c_1} is established through TR1, R15 and TR3. I_{c_1} will set up a p.d. across R15 which will have the effect of biasing on TR2 and establishing a second current flow, I_{c_2} through R16 and TR2.

This latter current flow is entirely dependent upon the demand of the current generator which is varying the p.d. across R15 and thus TR2 may be said to track the demand of the current generator. The closer the matching of R15/R16 and TR1 and TR2, the better will be the tracking and the better the symmetry of the integrator output waveform. Thermal stability is not a problem with TR1 and TR2 since the arrangement gives an equal and opposite reaction between these transistors for any variation in temperature.

I_{c_2} causes the integrator to ramp negatively and at a predetermined negative level IC4 will switch negative and IC5 positive. Thus TR3 and TR4 are now off and on respectively and since TR3 is off so also is TR2 and the current generator now discharges C1 via TR4 at a constant rate. The integrator will thus ramp positively until the switching point of IC4 is reached at which time the cycle repeats.

SINE WAVE SHAPER

The sine wave shaper used in the v.c.o. has been adapted from a design by D. T. Smith which appeared in *Wireless World* (Feb. 1973). Fig. 10.5 shows a detail of the circuit together with the waveforms presented at various points when the circuit is producing a sine wave having a low harmonic content.

The sine-shaper utilises the non-linear characteristics of a field-effect transistor in order to produce the desired output waveform and thus the operating points are quite critical. R20, 21 and D5, 6 provide a network which allows the gate to track the input signal and apply the necessary degree of "pinch-off" as the source signal approaches its maximum on both positive and negative half-cycles. Since the gain of the f.e.t. is changing continuously relative to the input signal the device may be considered to be operating in the ohmic region as a voltage variable resistor.

In Fig. 10.5 VR5 controls the d.c. offset of the input waveform and it is necessary to compensate for slight asymmetries which could be introduced in

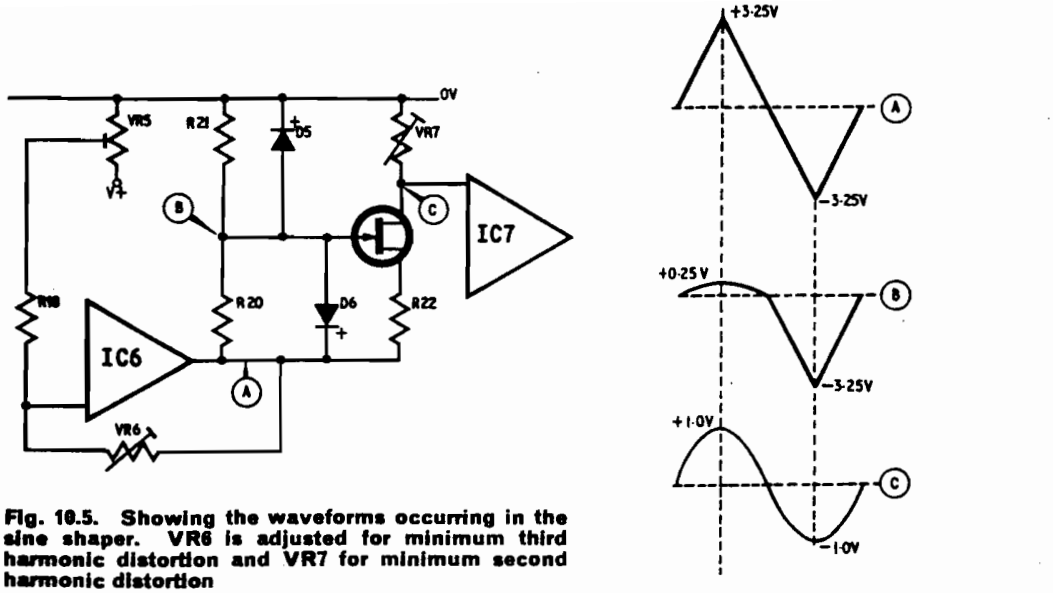


Fig. 10.5. Showing the waveforms occurring in the sine shaper. VR6 is adjusted for minimum third harmonic distortion and VR7 for minimum second harmonic distortion

the oscillator section. Over adjustment of VR5 in either direction can provide an alternative output waveform rich in harmonics.

VR6 sets the input signal level to the network. Too low a setting and the output waveform will be triangular while too much gain will give a waveform which is virtually a rounded off trapezoid. Careful adjustment of VR6 enables third harmonic distortion on the output to be reduced to a minimum.

VR7 controls the output amplitude of the signal. Too great a setting and the sine wave will become peaky while too low a setting will result in a squat, flattened out, waveform. Thus VR7 may be considered to control the second harmonic level and should be adjusted to minimise this characteristic.

BUILDING THE OSCILLATORS

The theoretical circuit of the complete oscillator module is shown in Fig. 10.6 while the recommended circuit board layout is shown in Fig. 10.7. It is strongly urged that construction of the module follows the guidelines suggested otherwise the interdependance of some of the controls is likely to make the final setting-up something of a nightmare.

Construction should start with assembly of the transistor oven, differential input summers and current generators. R1 should be 470 kilohm and left with fairly long leads to facilitate exchange during the final setting-up. Position the temperature control, preset VR1 to the R3 end of its travel to ensure that the comparator goes negative and thus turns off Q1 when power is applied. R10 should then be temporarily linked to the 0V rail and a decision taken as to the fate of R11. This resistor is optional in that it may be utilised to provide a third controlling input to the v.c.o. or it may be omitted at this stage without affecting anything. However, if it is decided to include R11 for the purpose of possible future additions to the circuitry it is important to remember that its presence could possibly compromise the setting-up of the oscillator if certain precautions are not taken.

If a third programming signal is to arrive at the oscillator from a low impedance source such as the output of another operational amplifier it is important that R11 also be temporarily linked to the 0V rail. Alternatively R11 may be left open circuit with the idea of using it only for the provision of occasional programming signals during which the tuning of the oscillator will have to be adjusted by means of VR4. In the setting-up instructions which follow R11 is open circuit.

SETTING UP

Since only one current generator can be set-up at a time the base of the second one (Q5) should be temporarily linked to the −15V rail to reduce the possibility of accidents. Set VR3 so that its value is 530 ohms. Note that if the positive lead of the ohmmeter is coupled to the −15V rail for this measurement the reading will not be compromised by the forward conduction of Q4. Set VR2 to the R6 end of its travel to ensure the minimum forward bias of Q4.

Set VR4 to its minimum setting and connect a milliammeter between the collector of Q4 and the 0V rail as shown in Fig. 10.8. As a safety precaution set the milliammeter to the 25mA range to start with. If the wiring up has been correctly carried out the milliammeter will show no reading when power is applied. On the other hand if the base of Q4 is incorrectly biased towards the positive region Q4 will pass a large current on switch-on which, besides possibly destroying the transistor, could also damage the meter.

Apply power and if no meter movement is observed reset to the 1mA range. Again there should be no obvious reading. Adjust VR2 towards the R5 end until the pointer of the meter makes a definite upward movement. At this point swing VR4 carefully over its full range and observe the maximum current drawn through Q4. The actual figure can vary quite widely at this stage and will probably be in the region 0·25–0·75mA.

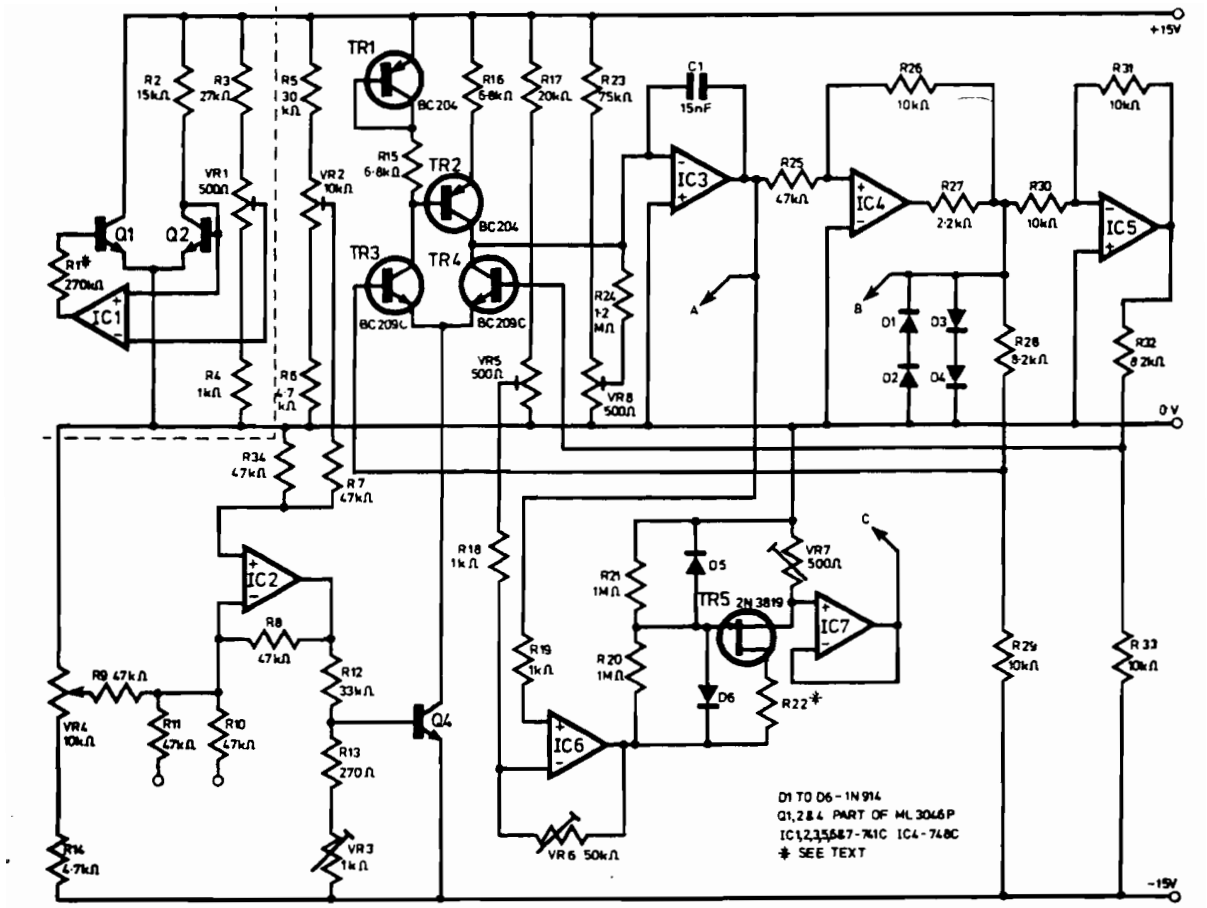


Fig. 10.6. Circuit of complete oscillator module. Points A, B and C are coupled to waveform selector switch

Set VR4 so that the meter is reading 0·2mA and place a slightly moistened finger on IC8—the transistor array. The meter reading should be seen to increase quite rapidly. Having made the above adjustments switch off and remove the meter from the collector circuit of Q4. Without disturbing the setting of any of the potentiometers temporarily link Q4 collector of the 0V rail. The same adjustments should now be made to the circuitry around Q5—having first removed the base/negative rail link.

In this case, however, leave the meter in circuit for the next stage of setting-up which entails fixing the thermal working points of the transistor oven.

Couple the oscilloscope to the output of the comparator IC1 which, at this point, will be about −14V. Carefully adjust VR1 until the comparator switches to +14V. At this time two things will start to happen. The first is that the meter will show a progressive increase in reading which, if the adjustment of VR1 has been made with care, should not exceed 1mA. The second is that within a second or so of the comparator switching positive the oscilloscope trace, which starts as a straight line, will begin to display a varying waveform.

At first the oscillation will zero about a point approximately 12V positive, but, as the chip temperature stabilises, the zero point will move down to about +6V to +9V. Monitor the base emitter voltage of Q2 which should be in the region 650mV to 680mV.

LOW LOAD POINT

At this time all four connected transistors are contributing towards the heating on the chip. Q1 with its 470 kilohms base resistor will be passing about 3mA and contributing about 45mW, Q2 in passing 1mA will be contributing about 15mW whilst Q4 and Q5 will be contributing about 6mW jointly. These latter devices, however, are passing considerably more current than they will be required to do when coupled to their respective oscillators and running at high frequency. It is therefore necessary to establish a low load set point to ensure that the oven maintains the same temperature over the full working range of the oscillators.

On both Q4 and Q5 reduce VR4 to its setting and readjust VR2 hard over towards R6—in other words reduce the forward bias on the transistors to the absolute minimum. These adjustments will cause

VOLTAGE CONTROLLED OSCILLATORS

COMPONENTS . . .

LOGARITHMIC V.C.O.s
(2 required)

Resistors
R1* 270kΩ (see text)
R2* 15kΩ
R3* 27kΩ
R4* 1kΩ
R5 30kΩ 2% metal oxide
R6 4·7kΩ 2% metal oxide
R7–R11 47kΩ (5 off) 2% metal oxide
R12 33kΩ 2% metal oxide
R13 270Ω 2% metal oxide
R14 4·7kΩ 2% metal oxide
R15–R16 6·8kΩ 2% metal oxide
R17 20kΩ
R18–R19 1kΩ (2 off)
R20–R21 1MΩ (2 off)
R22 See text
R23 75kΩ
R24 1·2MΩ
R25 47kΩ 2% metal oxide
R26 75kΩ 2% metal oxide
R27 2·2kΩ
R28 8·2kΩ
R29–R31 10kΩ (3 off)
R32 8·2kΩ
R33 10kΩ
R34 47kΩ 2% metal oxide

Capacitor
C1 15nF

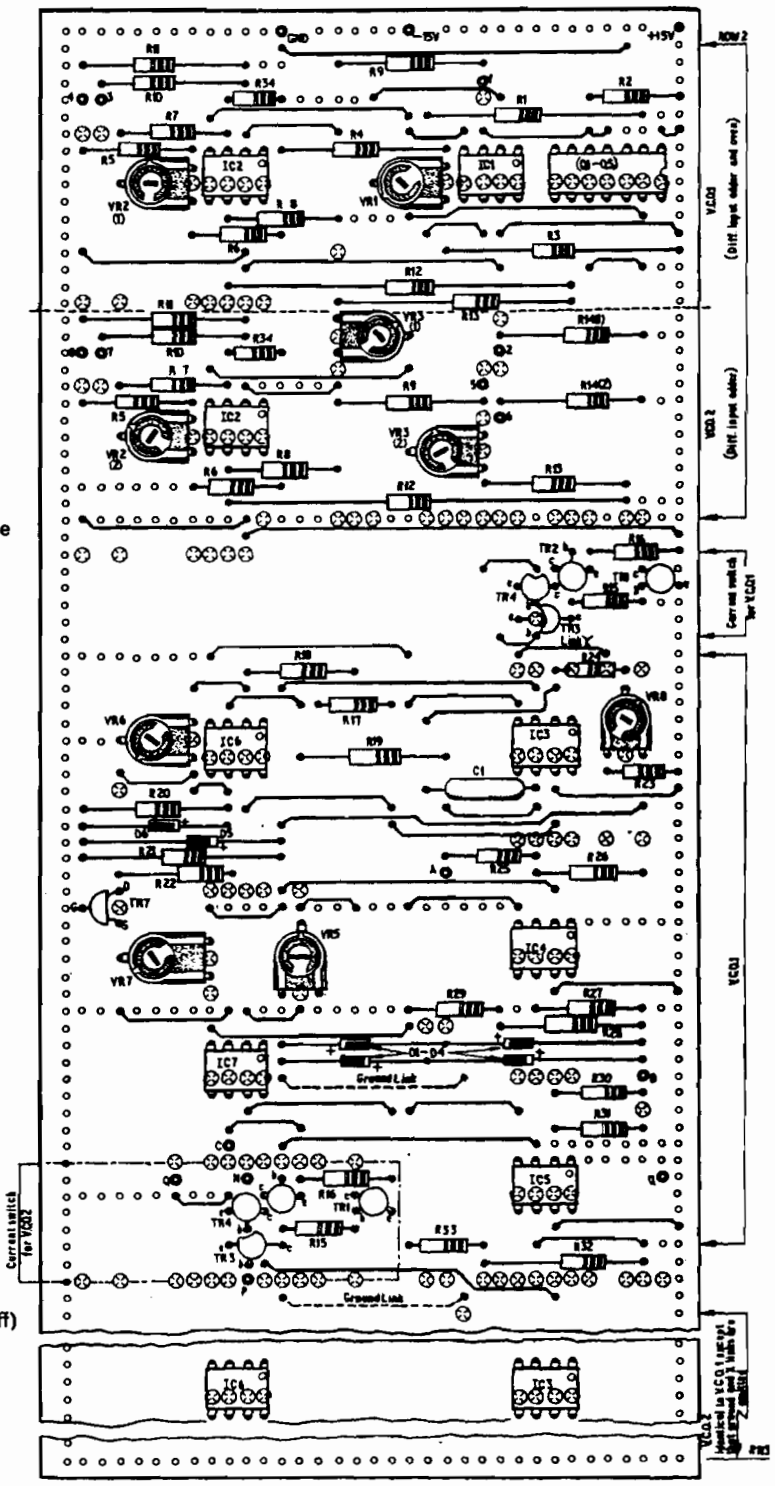
Potentiometers
VR1* 500Ω cermet preset
VR2 10kΩ cermet preset
VR3 1kΩ cermet preset
VR4 10kΩ midget moulded carbon
VR5 500Ω cermet preset
VR6 50kΩ cermet preset
VR7 500Ω cermet preset (see text)
VR8 500Ω cermet preset

Integrated Circuits
IC1* 741C
IC2, IC3, IC5, IC6, IC7 741C (5 off)
IC8* ML3046P (Q1, Q2, Q4, Q5)
IC4 748C

Transistors
TR1–TR2 BC204 (2 off)
TR3–TR4 BC209C (2 off)
TR5 2N3819

Diodes
D1–D6 IN914 (6 off)

Note: For components marked with an asterisk only 1 off is required.



1. Slider VR4 (1)
2. Hi-end VR4 (1)
3. R18 Control Input (1)
4. Spare Control Input (1)
5. Slider VR4 (2)
6. Hi-end VR4 (2)
7. R18 Control Input (2)
8. Spare Control Input (2)

Fig. 10.7. Board layout of oscillator module. Link point Q to Q. Link point N to junction of R33 and R33 on V.C.O.2. Link point P to junction of R28 and R29 on V.C.O.2

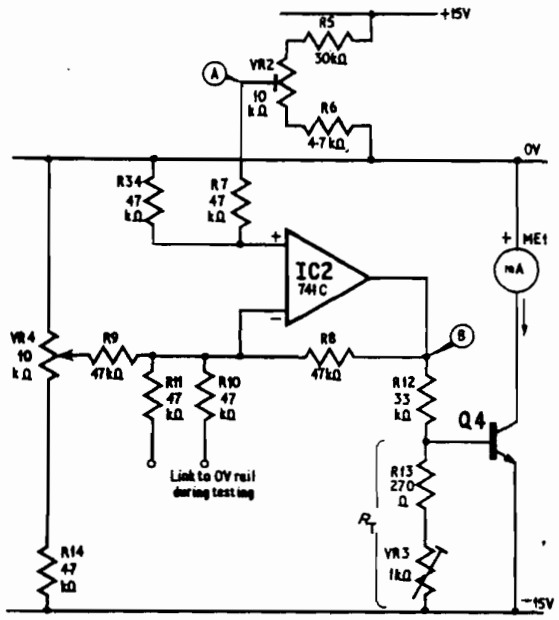
the oven temperature to fall and thus the comparator switching waveform will tend to move more positive and revert to a straight line trace.

Monitor the base/emitter voltage of Q2 again which, with the comparator positive, should not be greater than 680mV. If it is, or if, after a few seconds, the comparator waveform does not show signs of rippling, then the heat dissipation of Q1 is insufficient to maintain the set temperature. Much, of course, depends upon the ambient conditions when these measurements are being made and it is best to set up the low load point at the coolest temperature at which the v.c.o. is likely to be operated.

Under cool conditions therefore, if the comparator still does not ripple, it will be necessary to adjust the value of R1 to increase the current through Q1. In the prototype a value of 270 kilohms proved to be satisfactory and gave the desired comparator switching waveform at low load. The value of R1 is quite important because if it is too low the current switched by Q1 will be excessive and cause a considerable degree of jitter on the oscillator waveform.

Monitor $Q2V_{be}$ once more and adjust VR1 as necessary to bring the voltage to 680mV. All setting-up on the prototype oscillator was carried out at this value and it is important to bear in mind that the values of all subsequent measurements bear a close relation to this figure. If $Q2V_{be}$ is lower than 680mV this implies that the temperature of the oven is higher and thus Q4 will pass a higher current for any given value of control voltage. Since the frequency of the oscillator is linearly related to the current through Q4 then the frequency will also be higher.

The reverse will occur if the value of $Q2V_{be}$ is higher than the specified figure. However, for small variations from the specified value, the performance of the oscillator will still remain wholly logarithmic and sufficient tolerance has been allowed in the biasing control VR2 to compensate for such variations. Once satisfied that the upper and lower temperature set points have been correctly established VR1 may be locked with a small dab of non-conductive adhesive such as Araldite. Link the bases of Q4 and Q5 temporarily to the −15V rail.



V_{BE} Qz = 680mV: R_T = 750Ω

Bias Voltage "A"	Total Voltage "B" Bias + Control	Ic	V_{BE} (Q4) (mV)
2·74	2·74	12nA (calc)	395
2·74	5·75	160nA	461
2·74	7·76	600nA	500
2·74	8·76	1·5μA	528
2·74	9·76	3·7μA	550
2·74	10·78	7·0μA	570
2·74	11·78	20·0μA	595
2·74	12·78	41·0μA	617
2·74	14·39	60·0μA	630
	Referred to 0V Rail		Referred to −15V Rail

Fig. 10.8. Measurements of $Q4V_{be}$ made with Avo 8 which illustrate the degree of error that is possible when interpreting the reading

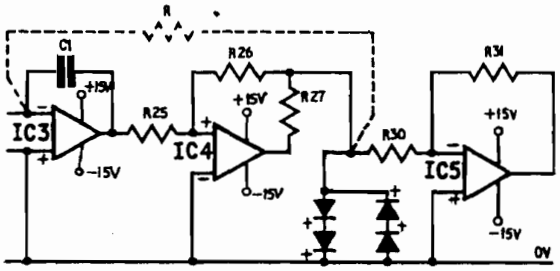


Fig. 10.9. Basic circuit elements of the oscillator and inverter (IC5). Resistor R is any value between 2kΩ and 1MΩ and is temporarily coupled as shown to prove oscillator function

PROVING THE OSCILLATORS

Fig. 10.9 shows the circuit elements involved in the construction of the oscillator section. When these items have been assembled temporarily connect a resistor of between 2 kilohm and 1 megohm from the junction of R27/R30 and the inverting input of IC3. With an oscilloscope monitoring the output of IC3 apply power and a triangular waveform will be observed at a frequency dependent upon the value of linking resistor chosen. Having proved the functioning of the oscillator assemble one current switch and couple to a current generator having first removed its base shorting link. Resistors R28/29 and R32/33 should be added at this time. The purpose of these resistors is to establish a negative bias point for transistors TR3 and TR4 in the

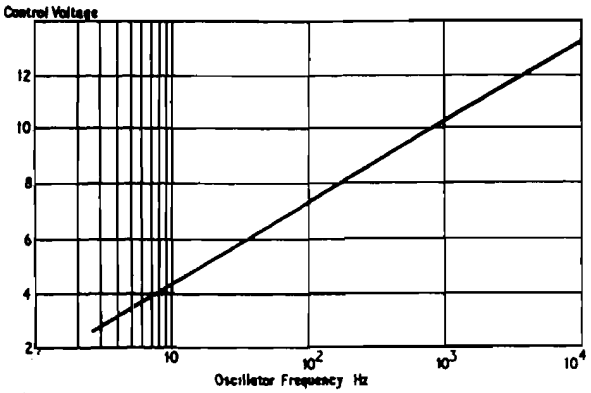


Fig. 10.10. Control voltage/frequency relationship

current switch and whereas the exact value of the resistors concerned is not entirely critical it is important that R28/32 and R29/33 be as closely matched as possible to ensure that the bias points of TR3 and TR4 are the same.

A quick check may now be made to ensure that the separate circuits work together as a complete unit. Remember to reset VR2 and VR4 to about mid position. Depending upon the setting of VR3 it is possible that rotation of VR4 will cause the oscillator to go into saturation towards either extremity but this is not important at this stage and will be dealt with during final setting up.

The next stage is to build the second oscillator following the same general pattern and, having established that it functions, begin the process of matching the performance. The closest possible matching of performance will be obtained if relatively close tolerance components have been used in the construction and, for this reason, 2 per cent resistors have been specified throughout. In particular it is prudent to obtain a matched pair of integrating capacitors (C1).

BIASING

Firstly it is necessary to establish a value of minimum bias on Q4 and Q5 which will support oscillation. Due to the inherently close electrical matching of the transistors on the 3046 the same level of bias will result in current flows through the transistors which are, for all practical purposes, identical. In the prototype it was found that the output of IC2 was at +2·74V referred to the OV rail for an oscillation frequency of 0·2Hz.

Set VR4 to its minimum position and adjust VR2 until the output voltage on IC2 (both oscillators) reaches +2·74V as above. Monitoring the integrator output waveform on both oscillators at the same time, if possible, adjust VR3 on Q4 and Q5 *with the greatest care* so that both oscillators are running at the same frequency—the exact rate is not critical. With VR4 still at its minimum setting apply an external control voltage to R10 on both oscillators at the same time having first broken the temporary link connecting R10 to the OV rail. A fresh 9V battery with a suitable potentiometer coupled across its terminals is ideal for the purpose of providing the control voltage.

Connect the positive end of the battery to the OV rail and the slider of the potentiometer to both R10's. With the slider hard negative monitor the output frequencies of both oscillators, preferably at the same time, and confirm that they are running at the same frequency which should be in the region of 3kHz. Note that since the oscillators are not phase locked a certain degree of drift between them is almost inevitable and it should be the aim to reduce the amount of drift, by adjustment of VR3, to within 1 per cent or better of the frequency being monitored. Thus for a frequency of 3kHz a drift of about 30Hz would be at the limits of acceptability. Compare frequencies at various settings of the potentiometer to ensure that the frequencies and drift relationships remain stable over the full range.

OFFSETTING SATURATION

If, at the minimum setting, either or both oscillators go into saturation due to the adjustments made to VR3 it will be necessary to establish a slightly higher bias point by re-adjustment of VR2 and then repeat the whole of the setting up procedure so far outlined. Careful adjustment will result in a pair of oscillators which track the control voltages very accurately. It should not be the aim to reduce the drift between the oscillators to a very low figure as the beat frequency introduced by a drift of 0·5 per cent to 1 per cent will add interest and colour to the sound when both oscillators are being programmed in harmony. On the other hand a very low beat frequency can add quite unpleasant characteristics to a sound.

When satisfied that the oscillators are tracking over the full range of the control potentiometer the control voltage measured at the output of IC2 should be plotted against the frequency of oscillation at various points in the range. Fig. 10.10 shows the result of plotting the performance of the prototype oscillators.

F.E.T. CHARACTERISTICS

Before beginning the assembly of the sine shaper it is necessary to determine the exact characteristics of the f.e.t. which is to be used in the circuit. The two operational parameters which require to be known are the saturation current (I_{DSS}) at zero gate bias and the gate bias required to reduce the current through the device to negligible proportions. Fig. 10.11a/b illustrates the methods of making the measurements specified. If a variable voltage source

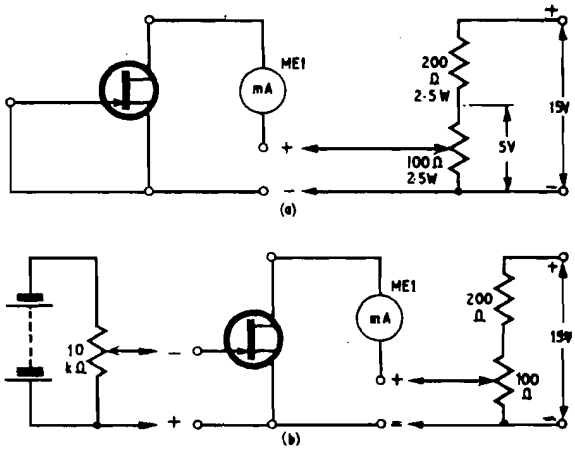


Fig. 10.11(a). Method for determining I_{DSS} at V_{GS}= O(b) method for determining V_{GS} when I_{DS}=O

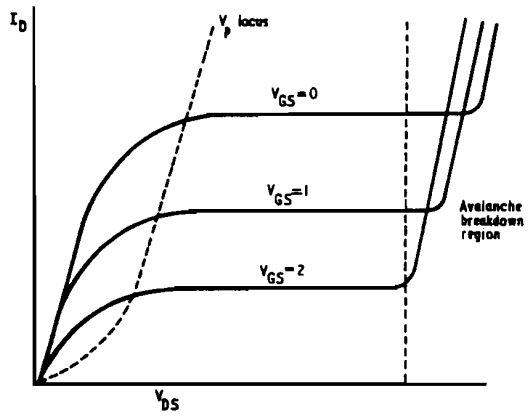


Fig. 10.12. Graph showing how V_p and I_{DSS} vary with V_{GS}

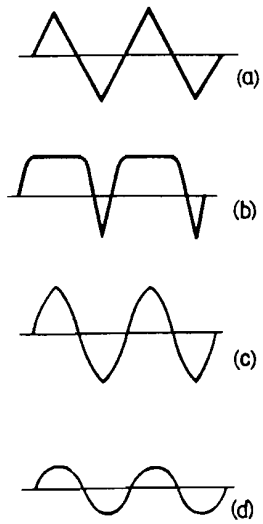


Fig. 10.13. Showing the effect on the sine shaper output waveform of adjustment of VR6 and VR7(a), VR6 too low (b), VR6 too high (c), VR7 too high (d), VR7 too low

is available it is preferable to use this in the source drain circuit rather than the divider arrangement illustrated and thereby gain the benefit of greater accuracy in the measurements.

The first stage is to measure the I_{DSS} at zero gate bias. With the variable voltage source at zero volts and the milliammeter on the 1mA range gradually increase the voltage setting, plotting, at various stages, the current/voltage relationship.

The point which is of interest is that at which further increases in voltage result in only a very small increase in current through the device. The voltage at which this phenomenon first occurs is known as the pinch-off voltage (V_p) and should be carefully recorded. After the pinch-off point has been reached the voltage may be increased quite significantly with very little increase in current until the avalanche breakdown region is reached. At this point the current through the f.e.t. will increase hugely and almost instantaneously and result in the destruction of the device. Hence the requirement to plot the measurements very carefully and note the point at which V_p is reached.

Fig. 10.12 shows a typical family of curves for any one f.e.t. and depicts the way in which the pinch-off voltage reduces as the gate bias is made progressively more negative with respect to the source. The next measurement to make therefore is the point at which the current through the f.e.t. reduces to negligible proportions and the set-up for doing this is illustrated in Fig. 10.11b. Having made the connections shown and with the 10 kilohm potentiometer wiper at the positive end of its travel adjust the variable voltage source so that the meter is indicating the I_{DSS}. At this point gradually advance the wiper and note that the meter reading reduces in proportion. Switch to a lower range on the meter as required and advance until the reading is zero. At this point carefully measure and note the voltage across the gate/source of the f.e.t.

The value of resistor R22 in the sine shaper is calculated on the basis of the readings above in the following way:—

$$R22 = \frac{V_p}{2.I_{DSS}}$$

The V_p in the above calculation refers to the value of gate/source voltage at which the current through the f.e.t. is zero. The value of the resistor will depend on the actual characteristics of individual f.e.t.s but would normally be expected to be quite small. In the prototype, for example, R22 was 180 ohms in one shaper and 270 ohms in the other. The value of VR7 should be chosen to provide a fairly wide margin of adjustment over the calculated value of R22 and in most cases a 500 ohm preset would be satisfactory.

ASSEMBLY

Having completed the above measurements the sine shaper can now be assembled. Bear in mind that f.e.t.s can be rather tricky to handle and it is a wise precaution to solder all the other components in position before actually inserting and fixing the f.e.t.

Setting-up the sine shaper consists of adjusting the values of VR5, 6 and 7 to provide the optimum sine wave. With power on adjust VR4 so that the oscillator is running at about 3kHz and monitor the output of IC7. The preset adjustments should be made with reference to Fig. 10.13 which illustrates the various waveform characteristics associated with these controls.

If a sine-wave oscillator is available it is helpful to compare the output of the shaper with a "genuine" sine wave of the same frequency. The scale of the waveform on the oscilloscope screen should be as large as possible for this purpose. This latter procedure was carried out with the prototype shapers and resulted in a sine wave output having a total harmonic distortion of only 1 per cent. A wave analyser or distortion meter if available could enable a higher purity sine wave to be obtained.

Next month: Envelope shaper, mixer networks and analogue memories for the keyboard unit.