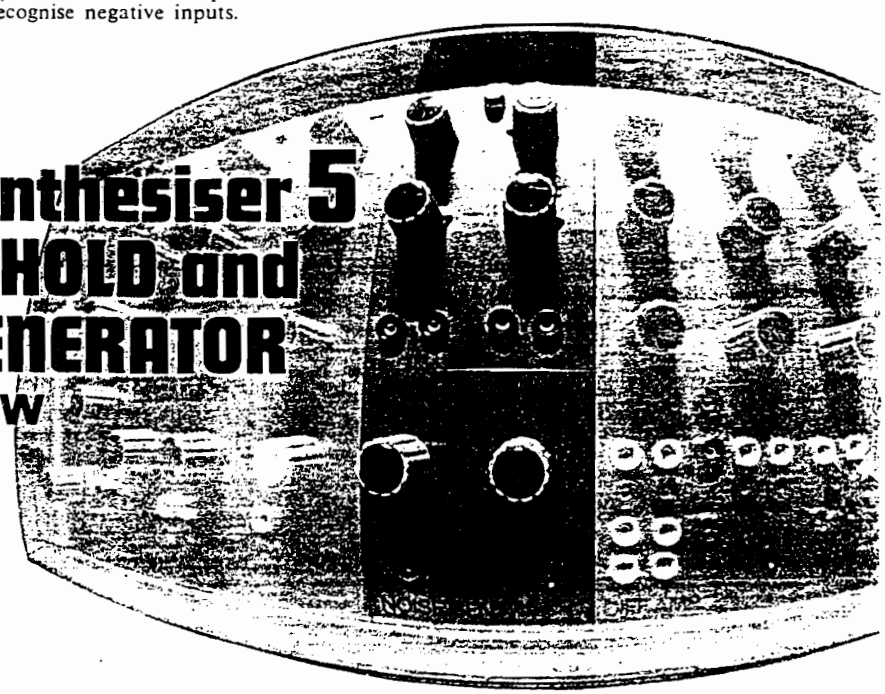
PE Sound Synthesiser 5
SAMPLE-HOLD and NOISE GENERATOR

By G.D. SHAW



THIS month the module containing the Sample and Hold circuitry and Noise Generator is described together with application details.

SAMPLE AND HOLD

The Sample and Hold shown in block form in Fig. 5.1 is another programming device which is capable of producing formalised staircase waveforms (Fig. 5.2) or random staircase waveforms. In both cases the "rise" of each step in the staircase is dependent upon the amplitude of the voltage being sampled while the "tread" of each step is governed by the sampling rate set by the clock.

The clock itself consists of two separate circuit forms as shown in the theoretical circuit diagram Fig. 5.3. The first is an astable multivibrator (IC1) in which the rate of oscillation is variable between 0·25Hz and 50Hz. The circuit switches alternately between its positive and negative saturation levels so that, for 15 volt supply rails, the output voltage swing is of the order of 28 volts.

The second circuit form is a monostable multivibrator (IC2) which is triggered by the negative going steps of the astable squarewave thus producing a pulse train of the same frequency. This circuit also switches between its positive and negative saturation levels. In the stable condition the output is positive. The introduction of a negative trigger pulse at the input, C3, causes the output to switch to its negative saturation level and to remain there for a period determined by the components R12 and C4.

PRECISION GATE

Clock pulses from the monostable are used to trigger an analogue gate (IC3) which has two summing inputs. One is coupled internally to a d.c. source and the other directly to an external sample socket. The gate will only recognise negative inputs. If the trigger input to the gate is left open circuit or is grounded the gate behaves like a unity gain inverter but only for negative going signals. A positive input signal would tend to swing the output of the gate negative, a tendency which is prevented by the bounding action of diodes D6 and D7.

Under normal conditions overriding control of the state of the gate depends upon the polarity of the signal presented at the trigger input. As has been explained, the gate is closed, that is, passing inverted negative signals, when the trigger input is open circuit or grounded. The same situation exists when the polarity of the trigger signal is negative.

When the trigger signal is positive however the gate opens and its output is zero *provided* that the potential of the sample input is less than the potential of the trigger signal. This latter situation exists for all conditions of internal sampling where the maximum d.c. level attainable is determined by the divider R26–VR4, and for all conditions of external sampling from a single programming source.

When the d.c. and external sampling sources are combined, providing a single programming source only is used, the maximum sampling potential will never exceed 11·5V as compared to a trigger potential of 14V, and thus the closed period of the gate will never exceed 560 microseconds.

In circumstances where two or more programming sources are combined either with, or without, amplification, the situation can exist where the sample potential exceeds the trigger potential. Under these conditions the closed period of the gate is solely dependent upon the period of "high" sample potential.

INTEGRATOR

Output from the gate is led to the programming input of an integrator/comparator (IC4/IC5) arrangement which is basically similar to the ramp generator described in last month's article. In this case, however, the time constant of the integrator is much shorter resulting in an extremely rapid integration.

This feature is necessary in order to provide the steep rise between steps if a crisp tone change is to be achieved.

Further additions to the basic ramp generator circuit include an indicator lamp switched by TR1 which serves to indicate the "on" period of the staircase, a clamping diode D1 which serves to limit the integrator output to approximately 650 millivolts in the event that the integrator tends to go into positive saturation, and an input bias control provided by R1, VR1, R2. Input bias is required to compensate for integrator capacitor leakage during the periods of hold between samples, particularly when the sampling rate is low. It also serves to allow the Sample and Hold to be used as another Ramp Generator if required. This is achieved by disabling the trigger socket (JK1) by the insertion of an open-circuit jack plug and setting the ramp rate by adjustment of the d.c. and bias controls. Very high ramp rates may be achieved by this means.

CONSTRUCTION

The circuit board layout of the Sample and Hold is shown in Fig. 5.4. Layout is not critical although space problems may occur if relative component

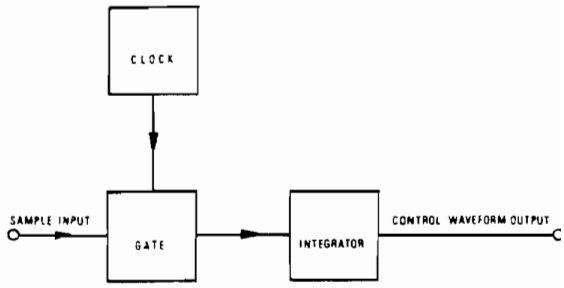


Fig. 5.1. Elements of Sample and Hold in block form

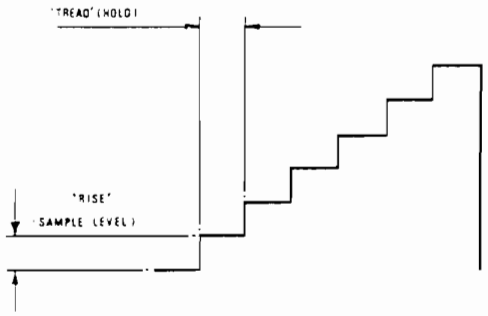


Fig. 5.2. Staircase waveform produced by Sample and Hold circuit. The rise of each step is dependent on the amplitude of the sampled voltage while the tread depends on the clock rate

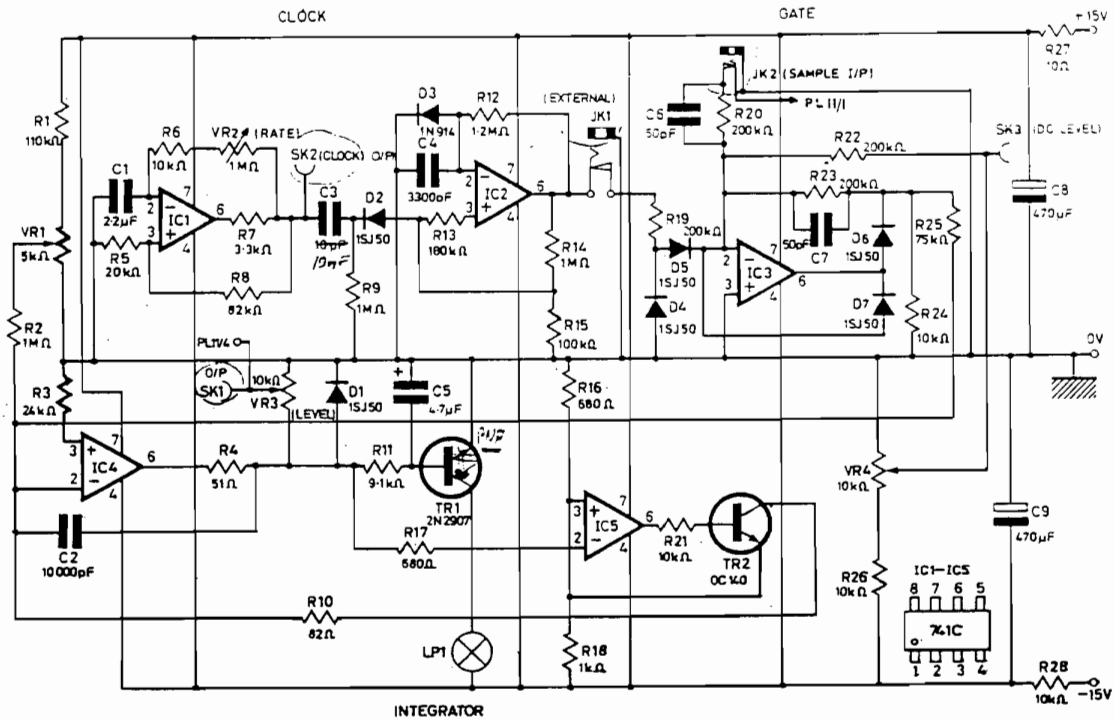


Fig. 5.3 Sample and Hold circuit

SAMPLE AND HOLD BOARD

COMPONENTS . . .

Resistors

R1	110kΩ	R15	100kΩ
R2	1MΩ	R16	680Ω
R3	24kΩ	R17	680Ω
R4	51Ω	R18	1kΩ
R5	20kΩ	R19	200kΩ
R6	10kΩ	R20	200kΩ
R7	3·3kΩ	R21	10kΩ
R8	82kΩ	R22	200kΩ
R9	1MΩ	R23	200kΩ
R10	82Ω	R24	10kΩ
R11	9·1kΩ	R25	75kΩ
R12	1·2MΩ	R26	10kΩ
R13	100kΩ	R27	10Ω
R14	1MΩ	R28	10Ω

All 5% ¼ watt carbon

Potentiometers

VR1	5kΩ lin. miniature moulded
VR2	1MΩ lin. miniature moulded
VR3–VR4	10kΩ lin. miniature moulded (2 off)

Transistors

TR1 2N2907
TR2 OC140

Capacitors

C1	2·2μF	35V Tantalum
C2	10,000pF	polystyrene
C3	10pF	polystyrene
C4	3,300pF	polystyrene
C5	4·7μF	40V tantalum
C6	50pF	polystyrene
C7	50pF	polystyrene
C8–C9	470μF	25V elect. (2 off)

Diodes

D1 ISJ50
D2 ISJ50
D3 IN914
D4–D7 ISJ50 (3 off)

Integrated Circuit

IC1–IC5 741C (5 off)

Miscellaneous

LP1–28V sub-miniature indicator lamp
SK1–SK3 2mm miniature sockets (3 off)
JK1, JK2 3·5mm jack socket (2 off)
0·1in matrix Veroboards as required

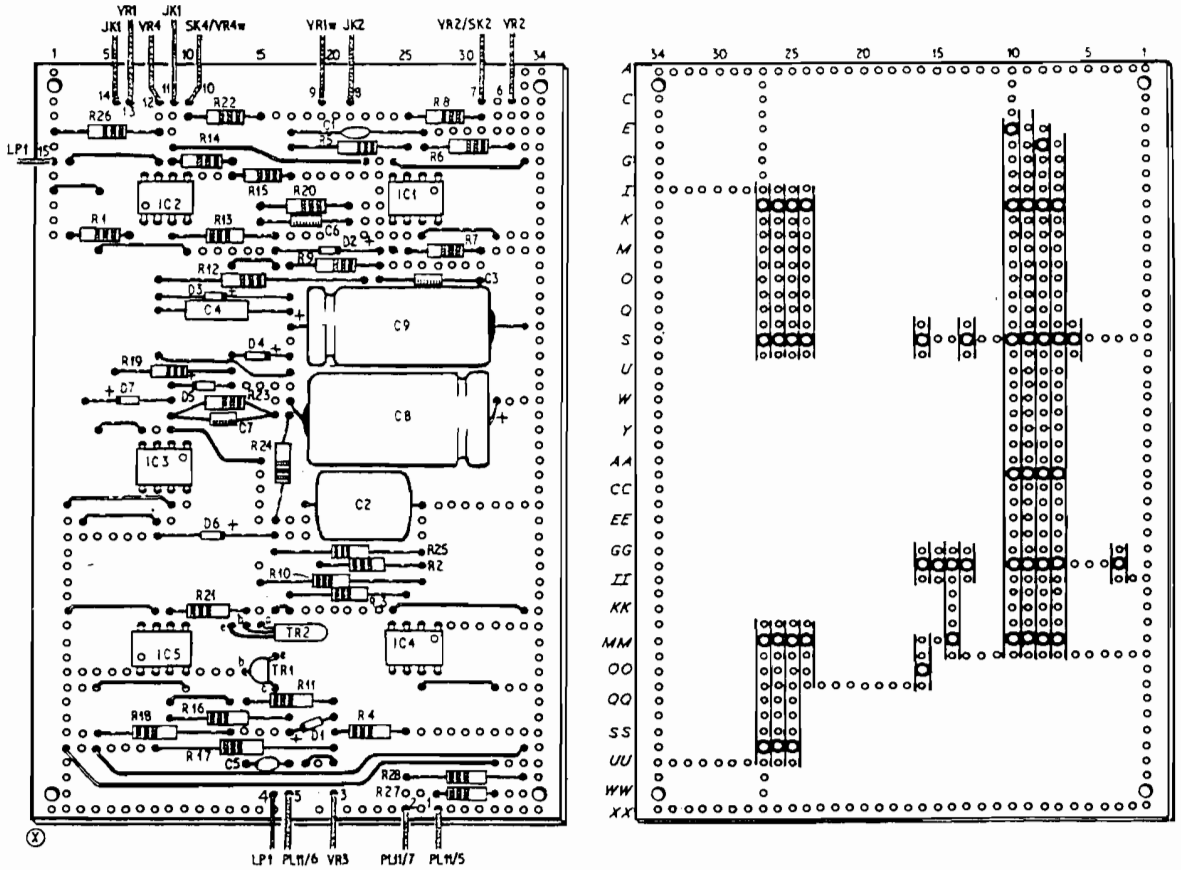


Fig. 5.4. Component layout and wiring of Sample and Hold Board

sizing differs appreciably from those shown. The power supply decoupling electrolytics present the biggest hazard as far as cramping of the board is concerned and these components should not be larger than 32mm in length by 16mm in diameter. R.S. Components Tube type are suitable and comply with the dimensions given.

EXPERIMENTAL CIRCUITS

The Sample and Hold provides the principal means by which the Synthesiser offers its most fascinating feature, that of "playing" by itself. Coupling the output to a v.c.o. and careful adjustment of the sample sources can provide a range of repetitive tone sequences the repeat period of which may be varied from a few seconds to several minutes.

Whether the sequence is truly repetitive or entirely random depends very largely on the choice of sample source. An article in the February issue of Hi-Fi News reviewed a recently issued record in which the "music" had been derived from computer stored data relating to changes in the Earth's magnetic field measured at a series of selected points.

In a similar manner existing data sources may be used to provide sample information. Crystal clocks, binary counters, ring counters, old non-erased computer tape and other digital data sources of various kinds, signal generators—even legitimate recorded music may be pressed into service, amplified, attenuated and blended together in various ways to serve the cause of random programming.

The discerning constructor will have noted that whatever the source of sample information the overall effect of the Sample and Hold is to turn this into a voltage which is progressively increasing, in steps, to a predetermined level at which point it returns to zero only to commence climbing once again. In practice the feature of a regular return to zero of the Sample and Hold output does not become obtrusive except at relatively slow sampling rates when the sample voltage shows very little variation between successive samples.

NOISE GENERATOR

White noise, defined in some circles as unwanted sound, is a very useful addition to the aural facilities provided by the synthesiser. It is a known fact that a great many sounds otherwise considered to be "pure" actually contain a relatively high noise content. The edge-tone in a wind organ is a typical example.

For imitative synthesis the addition of noise in greater or lesser degree is essential if the greatest approach to realism is to be achieved. This factor applies particularly to the synthesis of naturally occurring sounds such as rainfall, surf on the beach, storms, etc., and also to certain man-made sounds such as gunfire, explosions, train whistles, steam engines and so on.

Fig. 5.5 shows the theoretical circuit of the noise generator. The circuit is really quite simple. R5–R9; C3–C4 and D1 represent the noise generation section. The noise diode D1 is a specially selected noisy Zener marketed only by Semitron Ltd., and in the circuit configuration shown provides an output of about 75mV.

The noise bandwidth and level may be adjusted to a certain extent by varying the values of C4 and R6 respectively although it will be found, in practice, that the values shown are suitable for most purposes. C3 serves to decouple the noise diode from the inverting amplifier based around IC1.

Cost reduction can be achieved by omitting the offset adjustment preset VR3 and substituting a capacitor between the values of 0·01 and 0·1μF in the output of the operational amplifier as shown dotted.

LOW-PASS FILTER

R1, VR2 and C2 serve as a simple yet severe low-pass filter in order to provide a degree of control over the colouration of the noise. With VR2 at its minimum setting the output of the noise generator is reduced to a rough triangular waveform with a frequency in the region of 6kHz. Under these con-

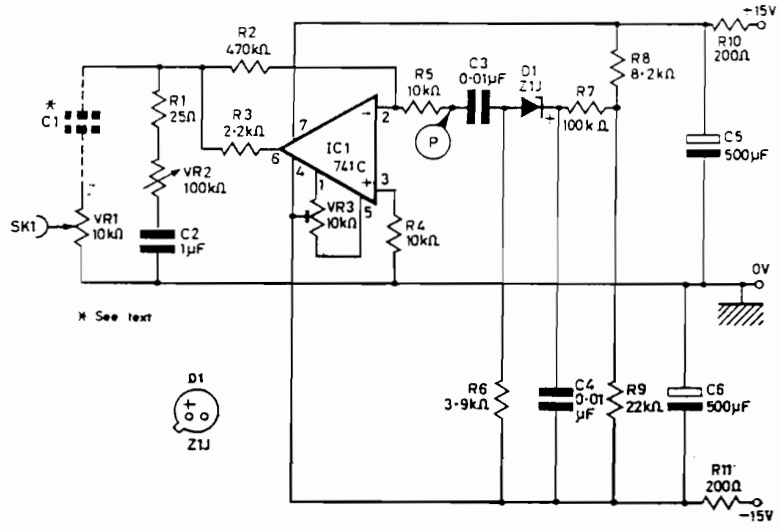


Fig. 5.5. Circuit diagram of Noise Generator

ditions the loading on the output of the operational amplifier is quite heavy and R3 is therefore included to limit the output current drain. Power supply decoupling is essential if noise is to be prevented from leaking back to the power distribution busbars.

In the circuit shown the current requirements are 2·5mA per rail and the addition of 200 ohm decoupling resistors will therefore result in a voltage drop of about 0·5V. If noise leak-through continues to be a problem these latter resistors may be increased in value quite considerably although if values over 500 ohms are used some adjustment of the values of R8 and R9 may be necessary to maintain their junction voltage at about +20V with respect to the negative rail.

Fig. 5.6 shows the circuit board layout of the noise generator. A piece of Veroboard or similar of 17 × 34 ways is suitable. Note that screened leads are used to connect this board's outputs with its associated components on the front panel. These leads should go direct to their respective components and not be bound into the wiring harness.

CONSTRUCTION

In general the construction of this module should follow the pattern adopted with those already described. The wiring harness for the Sample and Hold should pass out at the top of the front panel and down the length of the circuit board support plate to join the circuit board which is mounted adjacent to the McMurdo plug. The noise generator circuit board should be mounted over the lower pair of supports adjacent to the base of the front panel. Details of the front panel layout and module wiring are given in Fig. 5.7

SETTING-UP

It is recommended that setting-up and testing be established as a continuing process during construction of this module. With the noise generator, for example, it is suggested that the noise generating section consisting of R5–R9; C3–C4 and D1 be built first and tested by making temporary connections to the power supply rails and observing the output by connecting an oscilloscope between point "P" and the negative rail.

The expected output of the noise amplifier can be calculated at this stage by measuring the noise output of the diode with respect to signal ground and multiplying this by the gain of the amplifier.

In the prototype the total noise output was 3·5V maximum which is more than adequate. If the performance of this stage is satisfactory construction of the amplifying section can go forward being similarly tested on completion and before mounting the finished board into the module.

There is no actual "setting-up" to be done with the Sample and Hold and the purpose of testing is merely to establish that the circuit performs within the previously described limits.

NOISE GENERATOR BOARD

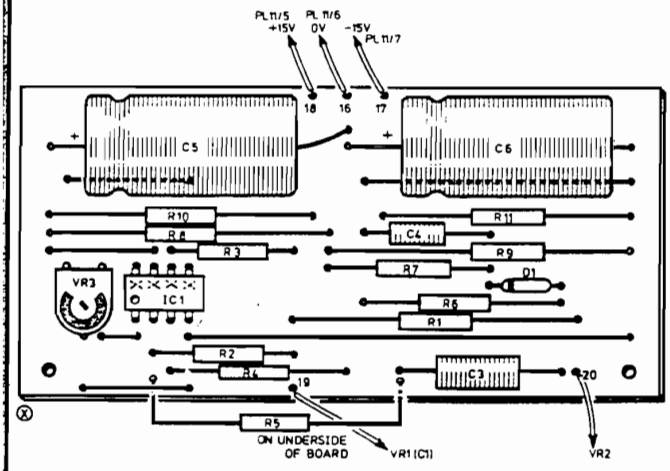


Fig. 5.6. Board layout and wiring for Noise Generator

COMPONENTS . . .

Resistors

R1	25Ω	R5	10kΩ	R9	22kΩ
R2	470kΩ	R6	3·9kΩ	R10	200Ω
R3	2·2kΩ	R7	100kΩ	R11	200Ω
R4	10kΩ	R8	8·2kΩ		

All ¼ watt 5% carbon

Capacitors

C1*	See text
C2	1μF polyester
C3	0·01μF
C4	0·01μF
C5	500μF elect. 16V
C6	500μF elect. 16V

Diode

D1 Z1J Zener (Semitron Ltd)

Potentiometers

VR1	10kΩ lin. miniature moulded
VR2	100kΩ lin. miniature moulded
VR3	10kΩ lin. horizontal carbon preset

Integrated Circuit

IC1 741C

Miscellaneous

SK1 2mm miniature socket
0·1in Veroboard as required

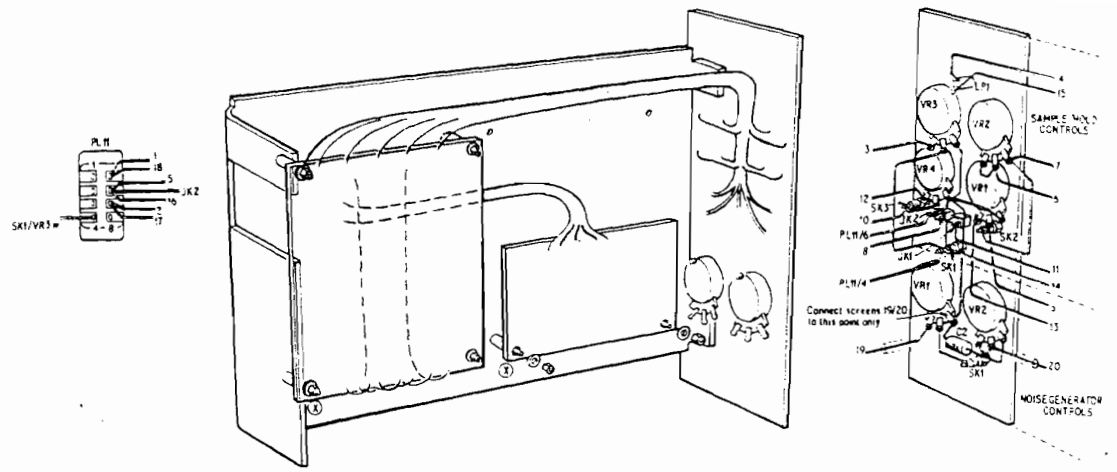


Fig. 5.7. Front panel component assembly with details of mounting and disposition of board on the module support plate. The small ringed X on the board edges indicates orientation. (See board assembly figures) For direct programming from the v.c.o. module connect SK11/4 to SK8/2

USING THE SAMPLE AND HOLD

It is best to confine initial experiments with the Sample and Hold to the formation of relatively simple staircase patterns, derived from the sampling of fixed d.c. voltages, in order to become familiarised with the effect of the adjustment of the various controls. Adjustment of the bias control, for example, can be quite critical when slow sample rates are being used and it is helpful to observe the output waveform on the oscilloscope so that drift between successive samples can be more easily balanced out.

When the Sample and Hold is programming a v.c.o. changes in "tread" voltage can be clearly discerned by ear but this becomes progressively more difficult as the sampling rate is increased. Note that it is difficult, if not impossible, to eliminate drift on the first step of a multi-step staircase due to the low charge on the integrating capacitor. This is not necessarily a disadvantage since it is possible to programme out the first step of the staircase by means of the envelope shaper which is to be described in a future article.

Progression to the sampling of varying voltages is the next logical step. Fig. 5.8 shows the effect of sampling a negative ramp having a period of about 0·1Hz. Note how the "rise" between "treads" increases in proportion to the increase in the ramp voltage. Variation in the ramp level by means of the input amplifier can cause remarkable changes in the output rhythm. A low ramp level and rapid sampling rate gives rise to an arpeggio-like sound in which the separation between the first few "treads" is barely discernible.

A high ramp level, on the other hand, causes the output of the integrator to reach its reset point fairly rapidly but since the sampling is continuing on an ever increasing ramp level the next staircase will have fewer steps and reach its reset point even more quickly. If the second reset is still well within the ramp period the third staircase will demonstrate even fewer steps while the fourth and subsequent staircases may consist of only one step, i.e. a square wave.

Variation of the sample voltage (ramp level) and sampling rate can ring the changes over a very wide range and produce some very interesting results.

SAMPLING A POSITIVE RAMP

Fig. 5.9 illustrates the effect of sampling a positive going ramp. In this case an initial condition of sampling fixed d.c. should be set and the ramp level adjusted so as not to exceed the d.c. sample voltage.

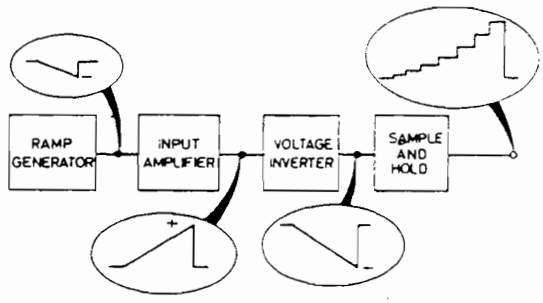


Fig. 5.8. Variable voltage programming. Note how the rise on consecutive steps at the output increase in proportion to the ramp level. Here d.c. level is zero

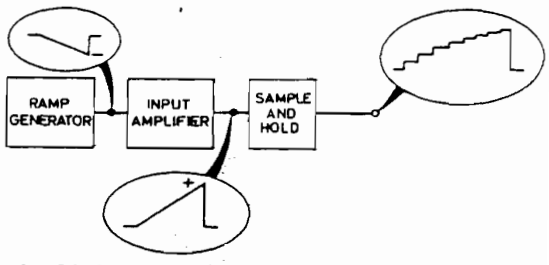


Fig. 5.9. Variable voltage programming. Here consecutive rises on the staircase output decrease with increase in ramp level. D.C. level is equal to or greater than the ramp level

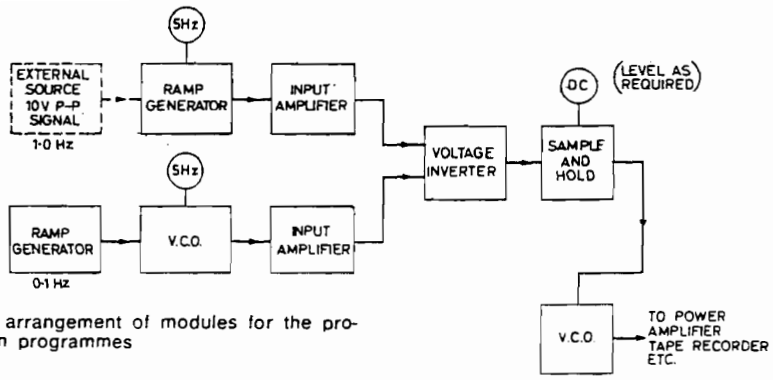


Fig. 5.10. Typical arrangement of modules for the production of random programmes

The effect of these settings is shown, i.e. a relatively large "rise" on the first few samples which gradually decreases as the ramp level rises. In other words a reversal of the situation illustrated in Fig. 5.8.

FURTHER EXPERIMENTS

Further experiments may be carried out in which the sample voltage is derived from two or more sources simultaneously and a typical arrangement is shown in Fig. 5.10.

The sample sources used need not, of course, be centred within the Synthesiser itself. Almost any device producing a varying output voltage may be used providing that the voltage amplitude concerned is compatible with the devices used in the synthesiser.

The output from a pick-up cartridge, tape recorder or radio can be amplified to a suitable level and used as sample material. Music which has wide and fairly rapid changes in dynamic range gives the best results.

Next month: Some general views on the establishment of an experimental sound studio and the construction of the Tone Control module will be described.